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Joshi et al.

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(54) **NON-PLANAR TRANSISTORS AND METHODS OF FABRICATION THEREOF**

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H01L 29/78 (2006.01)

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CPC ***H01L 29/66795*** (2013.01); ***H01L 29/6653*** (2013.01); ***H01L 29/66803*** (2013.01); ***H01L 29/785*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 29/66795
See application file for complete search history.

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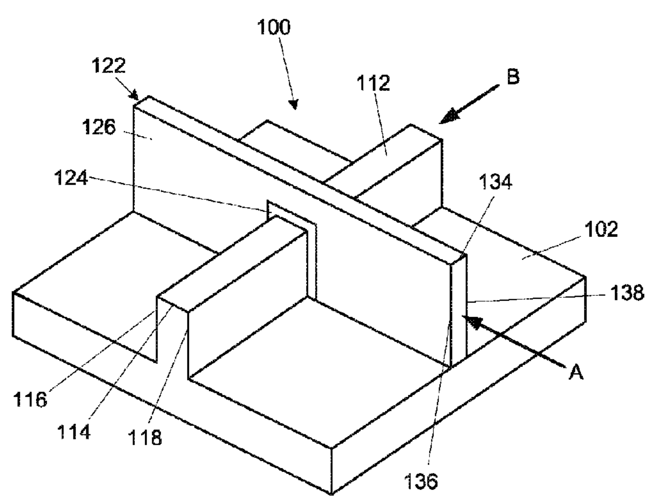
(74) *Attorney, Agent, or Firm* — Winkle, PLLC

(57) **ABSTRACT**

The present description relates to the formation source/drain structures within non-planar transistors, wherein fin spacers are removed from the non-planar transistors in order to form the source/drain structures from the non-planar transistor fins or to replace the non-planar transistor fins with appropriate materials to form the source/drain structures.

9 Claims, 10 Drawing Sheets



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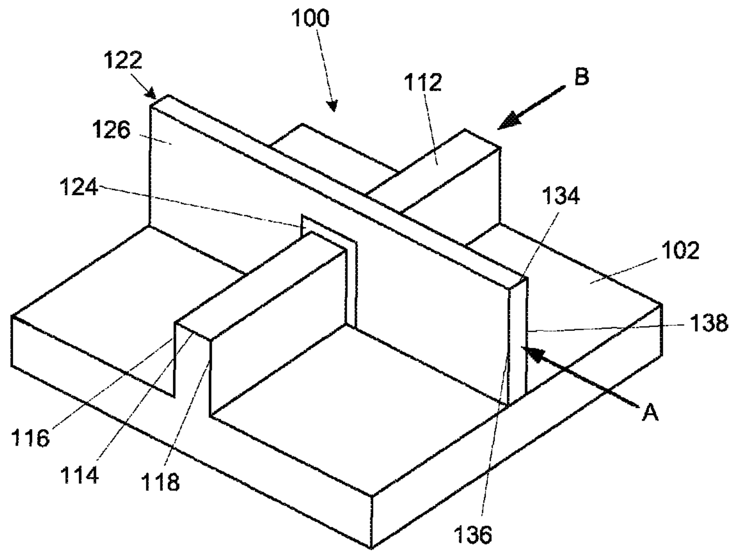

100
122
112
B
126
124
134
102
138
A
116
114
118
136

FIG. 1

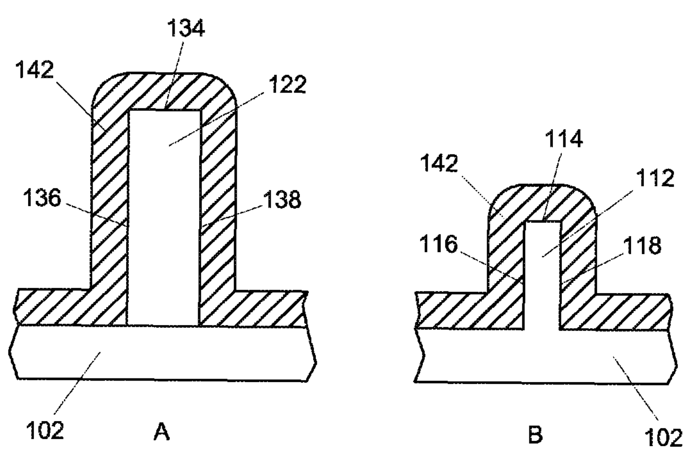

134
142
122
136
138
102
A
114
142
112
116
118
B
102

FIG. 2

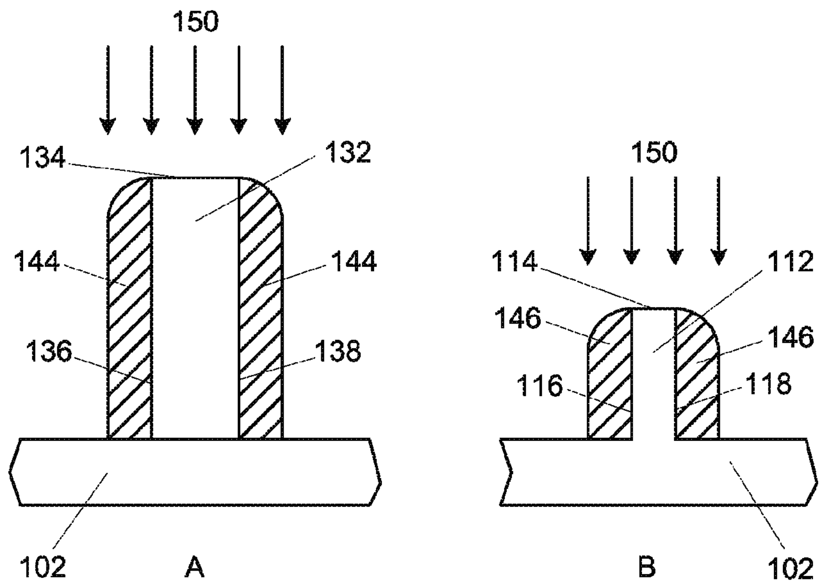

150
134
132
144
144
136
138
102
A
150
114
112
146
146
116
118
B
102

FIG. 3

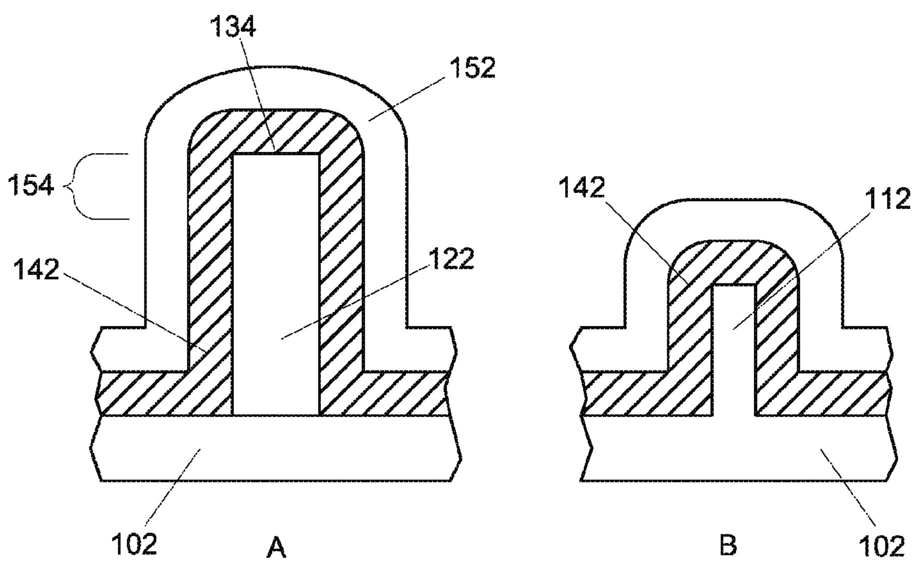

134
152
154
142
122
142
112
102
A
B
102

FIG. 4

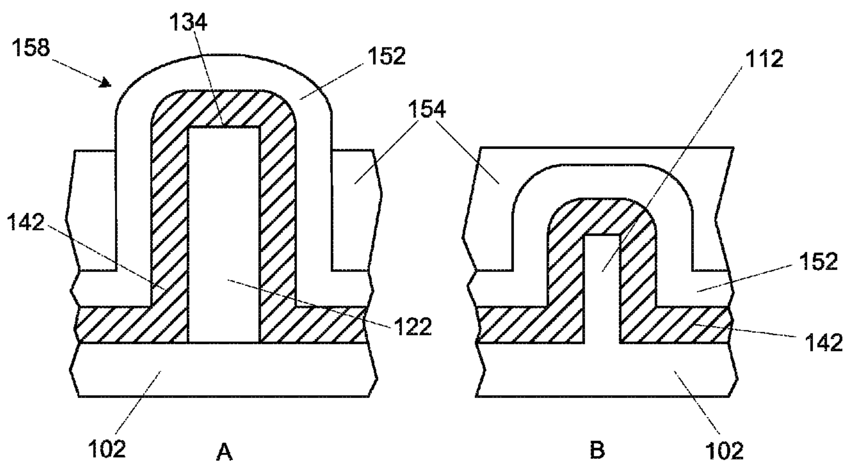

158
134
152
112
154
142
152
122
142
102
A
B
102

FIG. 5

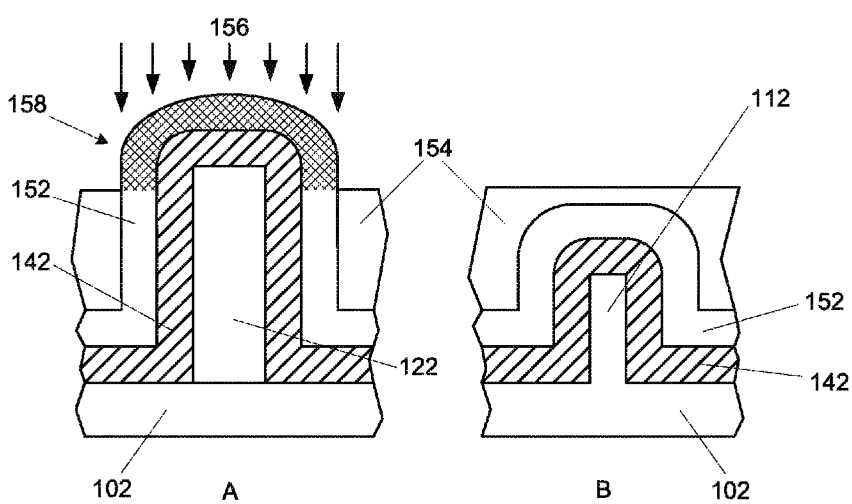
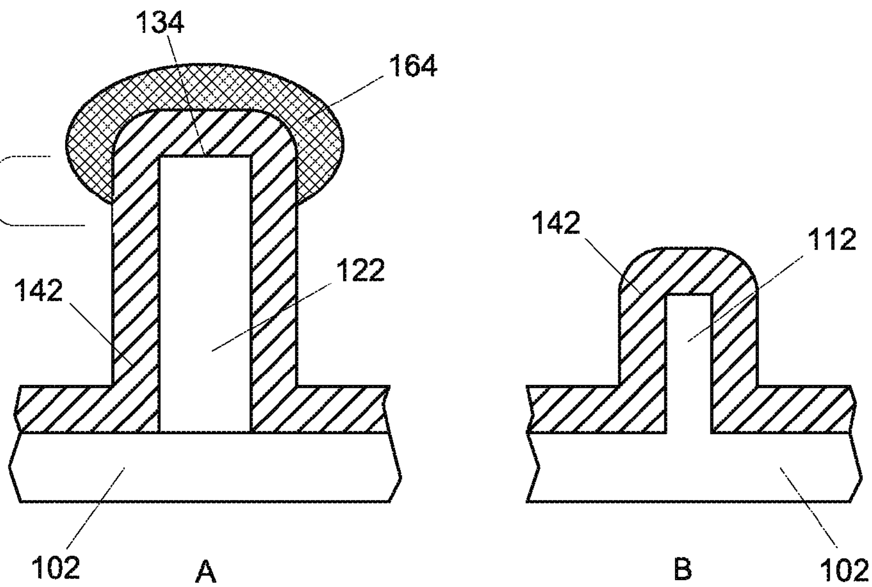
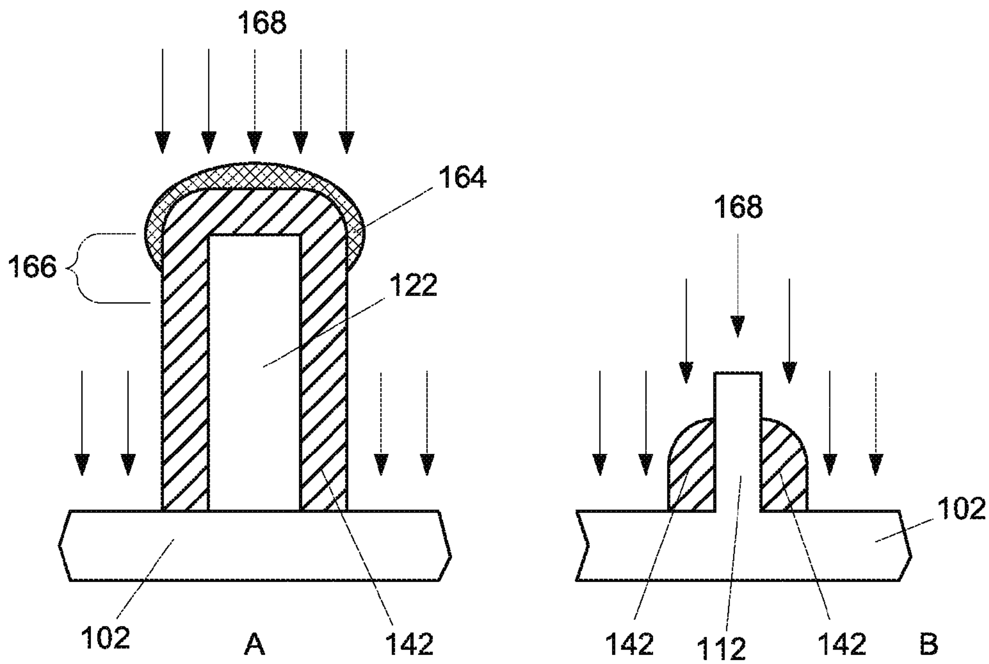

156
158
112
154
152
142
152
122
142
102
A
B
102

FIG. 6



134
164
166
142
112
142
122
102
A
B
102

FIG. 7



168
164
168
166
122
102
102
A
142
142
112
142
B

FIG. 8

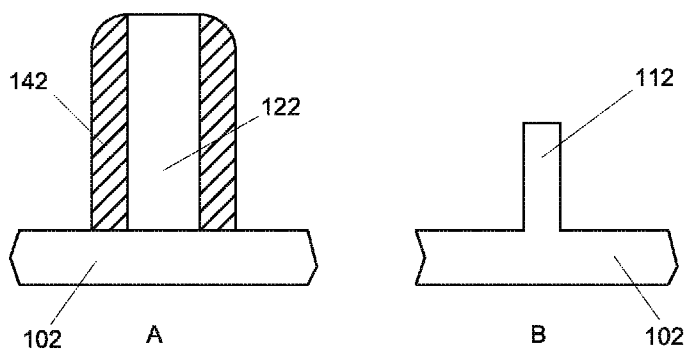


FIG. 9

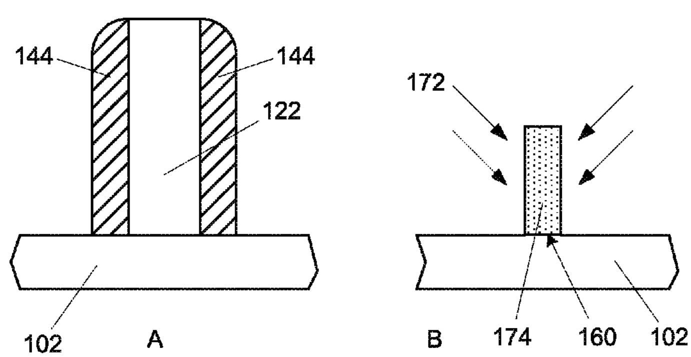


FIG. 10

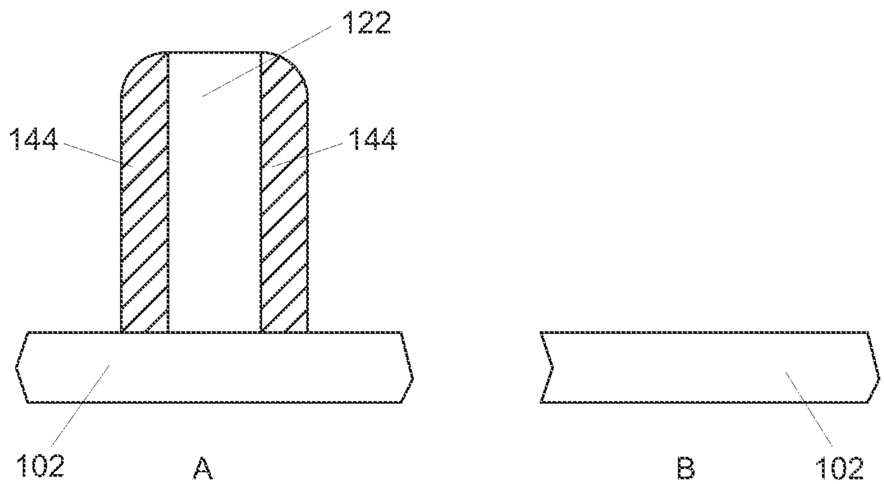


FIG. 11

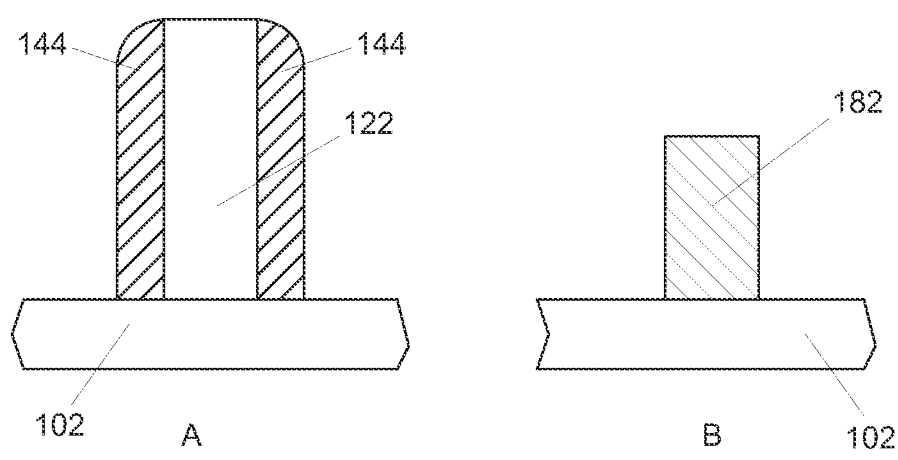


FIG. 12

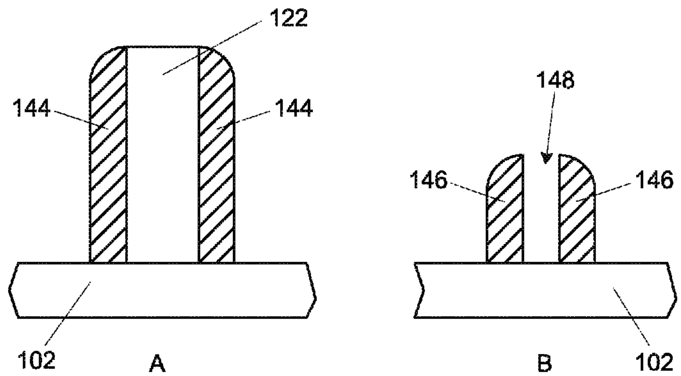

122
144
144
148
146
146
102
A
B
102

FIG. 13

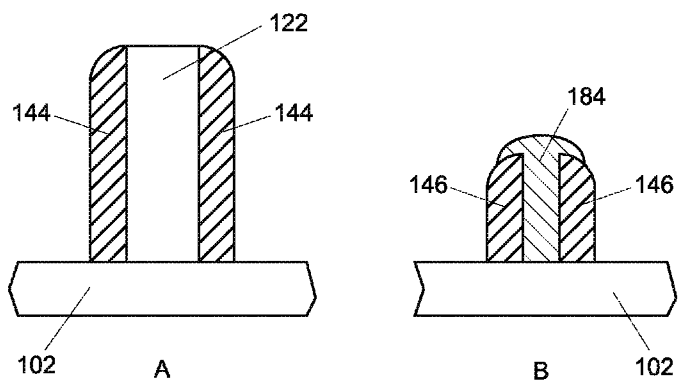

122
144
144
184
146
146
102
A
B
102

FIG. 14

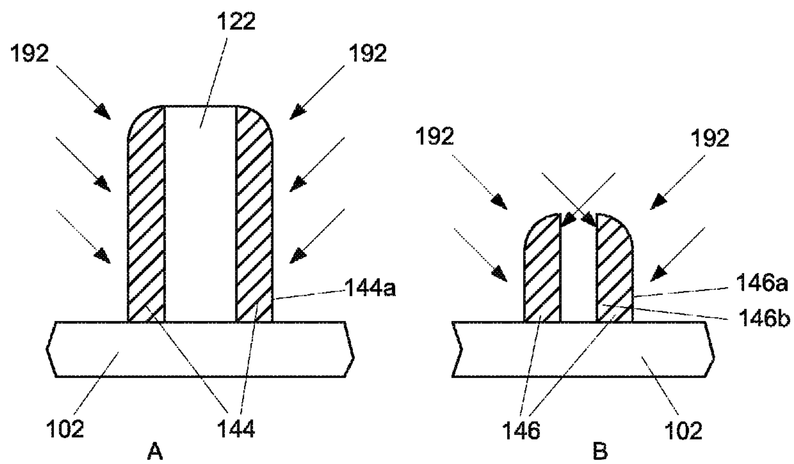

122
192
192
192
192
144a
146a
146b
102
144
146
102
A
B

FIG. 15

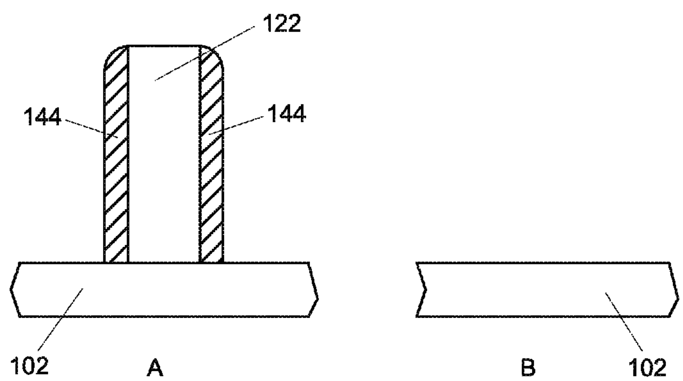

122
144
144
102
A
B
102

FIG. 16

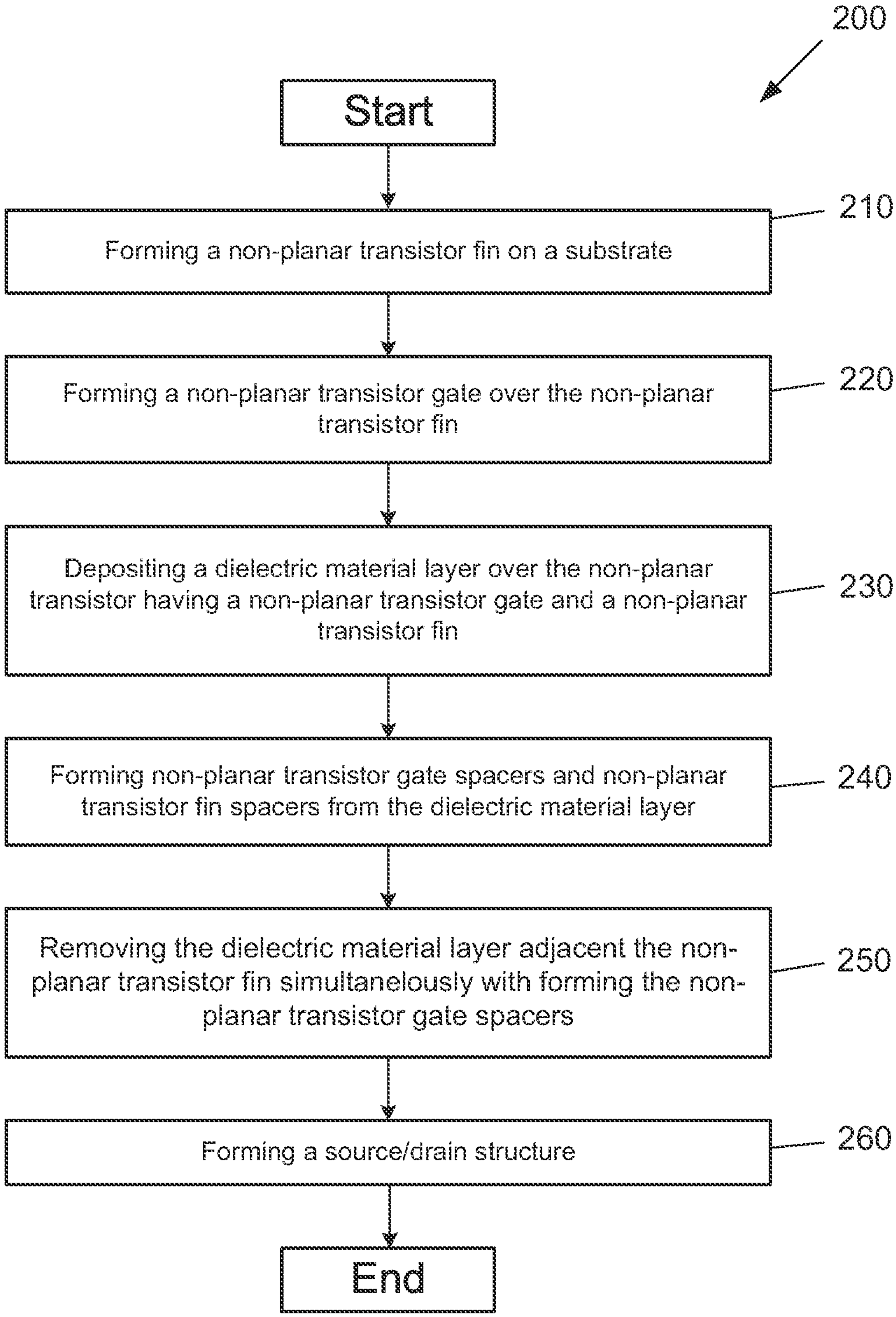

200
Start
Forming a non-planar transistor fin on a substrate
210
Forming a non-planar transistor gate over the non-planar transistor fin
220
Depositing a dielectric material layer over the non-planar transistor having a non-planar transistor gate and a non-planar transistor fin
230
Forming non-planar transistor gate spacers and non-planar transistor fin spacers from the dielectric material layer
240
Removing the dielectric material layer adjacent the non-planar transistor fin simultanelously with forming the non-planar transistor gate spacers
250
Forming a source/drain structure
260
End

FIG. 17

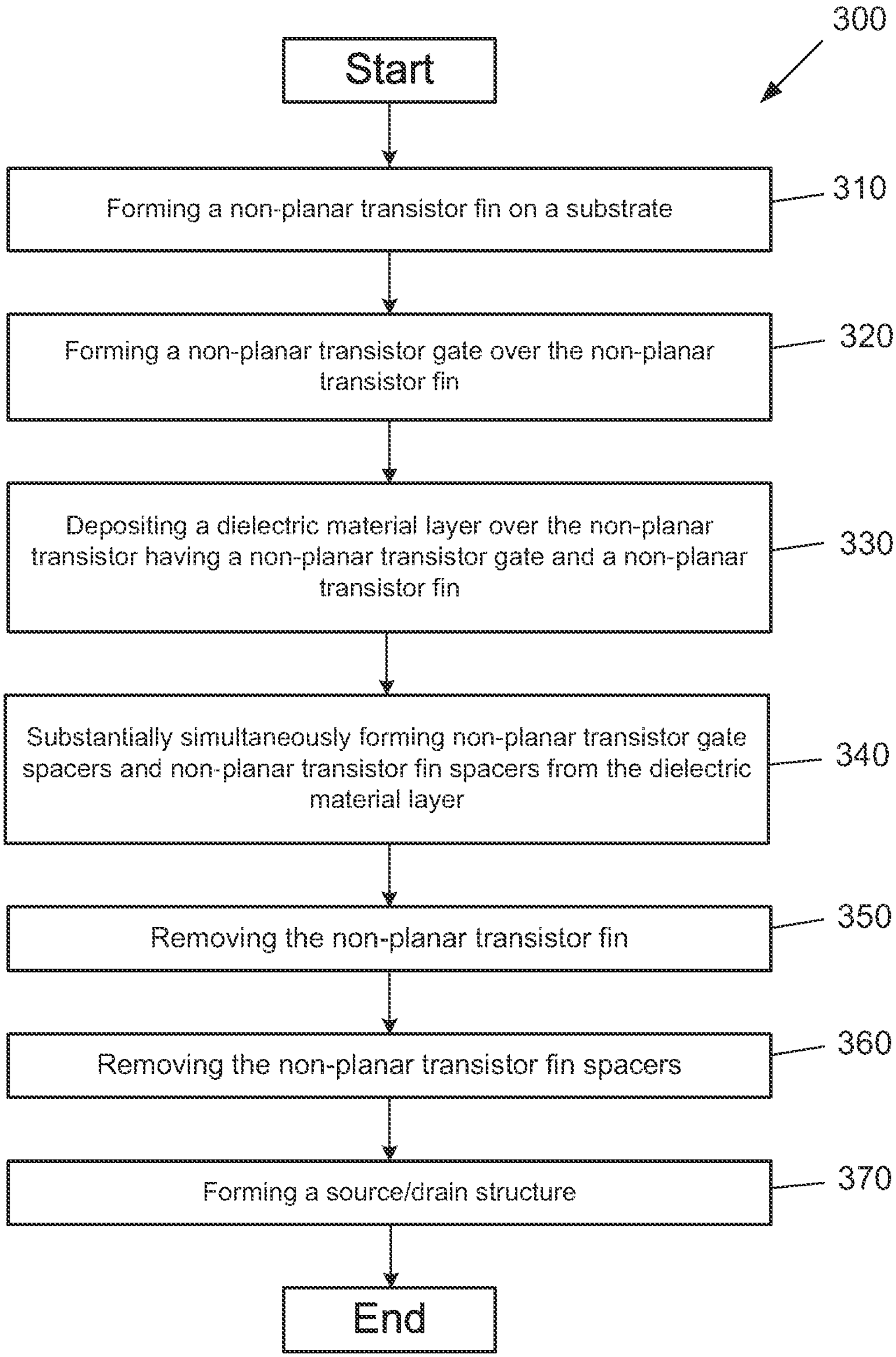

300
Start
Forming a non-planar transistor fin on a substrate
310
Forming a non-planar transistor gate over the non-planar transistor fin
320
Depositing a dielectric material layer over the non-planar transistor having a non-planar transistor gate and a non-planar transistor fin
330
Substantially simultaneously forming non-planar transistor gate spacers and non-planar transistor fin spacers from the dielectric material layer
340
Removing the non-planar transistor fin
350
Removing the non-planar transistor fin spacers
360
Forming a source/drain structure
370
End

FIG. 18

NON-PLANAR TRANSISTORS AND METHODS OF FABRICATION THEREOF

BACKGROUND

Embodiments of the present description generally relate to the field of microelectronic device fabrication and, more particularly, to the fabrication of non-planar transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. It is understood that the accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

FIG. **1** is a perspective view of a non-planar transistor structure, according to an embodiment of the present description.

FIG. **2** illustrates a side cross-sectional view of a dielectric material deposited over a transistor gate and a transistor fin of the non-planar transistor, according to an embodiment of the present description.

FIG. **3** illustrates a side cross-sectional view of the structure of FIG. **2** after the formation of transistor gate spacers and transistor fin spacers from the dielectric material on the transistor gate and the transistor.

FIG. **4** illustrates a side cross-sectional view of the structure of FIG. **2** after the formation of a capping material layer on the dielectric material, according to an embodiment of the present description.

FIG. **5** illustrates a side cross-sectional view of the structure of FIG. **4** after the formation of a sacrificial layer with a portion of the capping material layer expose, according to an embodiment of the present description.

FIG. **6** illustrates a side cross-sectional view of the structure of FIG. **5** after the alteration of the exposed capping material layer, according to an embodiment of the present description.

FIG. **7** illustrates a side cross-sectional view of the structure of FIG. **6**, wherein a capping structure is formed from the on the dielectric material on the transistor gate, according to an embodiment of the present description.

FIG. **8** illustrates a side cross-sectional view of the structure of FIG. **7** during a directional etching process, according to an embodiment of the present description.

FIG. **9** illustrates a side cross-sectional view of the structure of FIG. **8** after the directional etching process, wherein the dielectric material remains on the transistor gate while the dielectric is removed from the transistor fin, according to an embodiment of the present description.

FIG. **10** illustrates implanting the fin of FIG. **9** with a dopant to form a source/drain structure, according to an embodiment of the present description.

FIG. **11** illustrates a side cross-sectional view of the structure of FIG. **9** after the removal of the transistor fin, according to an embodiment of the present description.

FIG. **12** illustrates a side cross-sectional view of a source/drain structure formed after the removal of the transistor fin, as shown in FIG. **11**, according to an embodiment of the present description.

FIG. **13** illustrates a side cross-sectional view of the structure of FIG. **3** after the removal of the transistor fin from between the transistor fin spacers to form an opening, according to an embodiment of the present description.

FIG. **14** illustrates a side cross-sectional view of the structure of FIG. **13** after the filling the opening between the transistor fin spacers with a source/drain material.

FIG. **15** illustrates a side cross-sectional view of the structure of FIG. **14** during the removal of the transistor fin spacers with non-directional etch, according to an embodiment of the present description.

FIG. **16** illustrates a side cross-sectional view of the structure of FIG. **15** after the removal of the transistor fin spacers with non-directional etch, according to an embodiment of the present description.

FIG. **17** is a flow diagram of a process of forming a source/drain structures without spacers, according to one embodiment of the present invention.

FIG. **18** is a flow diagram of a process of forming a source/drain structures without spacers, according to another embodiment of the present invention.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Therefore, the use of the phrase "one embodiment" or "in an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present description.

In the fabrication of non-planar transistors, such as tri-gate transistors and FinFETs, non-planar semiconductor bodies may be used to form transistors capable of full depletion with very small gate lengths (e.g., less than about 30 nm). These semiconductor bodies are generally fin-shaped and are, thus, generally referred to as transistor "fins". For example in a tri-gate transistor, the transistor fins have a top surface and two opposing sidewalls formed on bulk semiconductor substrate or a silicon-on-insulator substrate. A gate dielectric may be formed on the top surface and sidewalk of the semiconductor body and a gate electrode may be formed over the gate dielectric on the top surface of the semiconductor body and adjacent to the gate dielectric on the sidewalls of the semiconductor body. Thus, since the gate dielectric and the gate electrode are adjacent to three surfaces of the semiconductor body, three separate channels and gates are formed. As there are three separate channels formed, the semiconductor body can be fully depleted when the transistor is turned on. With regard to finFET transistors, the gate material and the electrode only contact the sidewalls of the semiconductor body, such that two separate channels are formed (rather than three in tri-gate transistors).

Embodiments of the present description relate to the formation source/drain structures within non-planar transistors, wherein fin spacers are removed from the non-planar transistors in order to form the source/drain structures from the non-planar transistor fins or to replace the non-planar transistor fins with appropriate materials to form the source/drain structures.

FIG. **1** is a perspective view of a non-planar transistor **100**, shown as a tri-gate transistor, consisting of at least one non-planar transistor **112** from on or from the substrate **102** and at least one non-planar transistor gate **122** formed over the non-planar transistor fin **112**. In an embodiment of the present disclosure, the substrate **102** may be a monocrystalline silicon substrate. The substrate **102** may also be other types of substrates, such as silicon-on-insulator ("SOI"), germanium, gallium arsenide, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, and the like, any of which may be combined with silicon.

As shown in FIG. **1**, the non-planar transistor fin **112** may have a top surface **114** and a pair of laterally opposite sidewalls, a first sidewall **116** and an opposing second sidewall **118**, and the non-planar transistor gate **122** may have a top surface **134** and a pair of laterally opposite sidewalk, a first sidewall **136** and an opposing second sidewall **138**. As further shown in FIG. **1**, the transistor gate **122** may be fabricated over the non-planar transistor fin **112** by forming gate dielectric layer **124** on or adjacent to the transistor fin top surface **114** and on or adjacent to the first transistor fin sidewalls **116** and the opposing second transistor fin sidewalk **118**. The gate electrode **126** may be formed on or adjacent the gate dielectric layer **124**. In one embodiment of the present disclosure, the transistor fin **112** run in a direction substantially perpendicular to the transistor gates **122**.

The gate dielectric layer **124** may be formed from any well-known gate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), silicon nitride (Si_3N_4), and high-k dielectric materials such as hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. Furthermore, the gate dielectric layer **124** can be formed by welt-known techniques, such as by depositing a gate electrode material, such as chemical vapor deposition ("CVD"), physical vapor deposition ("PVD"), atomic layer deposition ("ALD"), and then patterning the gate electrode material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

The gate electrode **126** can be formed of any suitable gate electrode material. In an embodiment of the present disclosure, the gate electrode **126** may be formed from materials that include, but are not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide, aluminum carbide, other metal carbides, metal nitrides, and metal oxides. Furthermore, the gate electrode **126** can be formed by well-known techniques, such as by blanket depositing a gate electrode material and then patterning the gate electrode material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

A source region and a drain region (not shown) may be formed on opposite sides of the gate electrode **126**. In one embodiment, the source and drain regions may be formed by doping the transistor fin **112**, as will be discussed. In another embodiment, the source and drain structures may be formed by removing portions of the transistor fin **112** and replacing these portions with appropriate material(s) to form the source and drain structures, as will be discussed.

FIGS. **2-13** illustrate side cross-section views of the non-planar transistor gate **122** of FIG. **1** along arrow A, and side cross-section views of the non-planar transistor fin **112** of FIG. **1** along arrow B.

As illustrated in FIG. **2**, a dielectric material layer **142** may be conformally deposited over the non-planar transistor **100** of FIG. **1** to cover the non-planar transistor gate **122** and the non-planar transistor fin **112**. As known to those skilled in the art, conformally deposited material has substantially the same thickness deposited on all exposed surfaces of the object being coated. The dielectric material layer **142** may be formed from any well-known gate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), silicon nitride (Si_3N_4), and high-k dielectric materials, which may be conformally deposited by any appropriate technique known in the art.

The dielectric material layer **142** of FIG. **2** may be etched by as directional etch (shown as arrows **150**) with an appropriate etchant and by any known technique to remove a portion of the dielectric material layer **142** proximate the non-planar transistor gate top surface **134** to form spacers **144** adjacent the non-planar transistor gate sidewalls **136** and **138** and simultaneously form spacers **146** on the non-planar transistor fin sidewalk **116** and **118**, while substantially removing the dielectric material layer **142** adjacent the substrate **102**, as shown in FIG. **3**. As known to those skilled in the art, directional etching may be conducted to etch a material along a specific axis. As further known to those skilled in the art, spacers (e.g. elements **144** and **146**) are thin dielectric material layers formed adjacent sidewall of conductive structures in microelectronic devices, such as transistors, to electrical isolate those conductive structures. Although the non-planar transistor gate spacers **144** are needed to define the separation of the non-planar transistor gate **122** from subsequently formed source and drain structures (hereinafter referred to collectively as "source/drain structures"), the formation of the non-planar transistor fin spacers **146** may interfere with desired definition and formation of source/drain structures or may interfere with desired modification of the non-planar transistor fin **112** into source/drain structures, as will be discussed.

FIGS. **4-9** illustrate one embodiment of a process for removing non-planar transistor fin spacers **146** without removing the non-planar transistor gate spacers **144**. As shown in FIG. **4**, a capping material layer **152**, such as a chemical vapor deposition formed layer of silicon dioxide, may be formed over the dielectric material layer **142**. As shown in FIG. **5**, a sacrificial layer **154** may be formed over the capping material layer **152**, and may be recessed to expose a portion **158** of the capping material layer **152**. The recessing of the sacrificial layer **154** may be achieved by any etching technique, such as a dry etch. As shown in FIG. **6**, the exposed portion **158** of the capping material layer **152** may be alter to change is etching characteristics, such as a high dose ion implant, shown as arrows **162**. With the high dose ion implant, the implant dose should be high enough to make a compositional change in the implanted portion of the capping material layer **152**. The sacrificial layer **154** may be removed, such as by ashing followed by a cleaning step, and a high temperature anneal (to incorporate the implanted ions), and the unaltered capping material **152** may be removed, such as by etching, to form a capping structure **164** proximate an upper portion **166** of the non-planar transistor gate **122** proximate the non-planar transistor gate top surface **134**, as shown in FIG. **7**. It is understood that the capping structure **164** may be any appropriate material, such as photoresist materials as will be understood to those skilled in the art.

As shown in FIG. **8**, a directional etch (illustrated by arrows **156**) may be performed on the dielectric material layer **142** to etch in a direction toward the substrate **102**. With such a directional etch **168**, the capping structure **164** protects the dielectric material layer **142** adjacent the non-planar transistor gate **122** while the dielectric material layer **142** adjacent the substrate **102** and the non-planar transistor fin **112**. This may result in a portion of the dielectric material layer **142** remaining adjacent non-planar transistor gate **122** with substantially all of the dielectric material layer **142** being removed from the non-planar transistor fin **112**, as shown in FIG. **9**. Once the portion of the dielectric material layer **142** has been removed from the non-planar transistor fin **112** at least a portion of the non-planar transistor fin **112** may be implanted with a dopant (shown with arrows **172**) to form a source/drain structure **174**, as shown in FIG. **10**. As will be understood to those skilled in that art, the dopant implantation is a process of introducing impurities into semiconducting materials for the purpose changing its conductivity and electronic properties. This is generally achieved by ion implantation of either P-type ions (e.g. boron) or N-type ions (e.g. phosphorous), collectively referred to as "dopants". As further shown in FIG. **10**, in order to achieve a uniform doping of the non-planar transistor fin **112**, the dopants may be implanted **172** into the transistor fin **112** at an angle from either side of the non-planar transistor fin **112**.

In another embodiment, the non-planar transistor fin **112** (see FIG. **9**) may be removed by any technique known in the art, such as etching, as shown in FIG. **11**. In one embodiment, the non-planar transistor fin **112** may be removed by a plasma etching process with gasses, such as hydrogen bromide, nitrogen trifluoride, and sulfur hexafluoride, or by a wet etch with solutions, such as ammonia hydroxide, potassium hydroxide, tetratmethylammonium hydroxide, and the like.

Once the non-planar transistor fin **112** has been removed, a source/drain structure **182** may be formed in its place, as shown in FIG. **12**. The source/drain structure **182** may be fabricated by any known fabrication processes, including but not limited to deposition, lithography, and etching processes. In one embodiment, the source/drain structure **182** may be epitaxially grown silicon, silicon germanium, silicon/germanium/tin, germanium, silicon carbide, and the like, and may include dopants, such as boron or phosphorus (as previously discussed). As will be understood to those skilled in the art, the material used in the fabrication of the source/drain structure **182** may be designed to have substantially optimal performance for the non-planar transistor **100** (see FIG. **1**) in which it is used.

In still another embodiment, beginning at FIG. **3**, the non-planar transistor fin **112** can be removed from between the non-planar transistor fin spacers **146** to form an opening **148** by any technique known in the art, such as etching, as shown in FIG. **13**. Once the non-planar transistor fin **112** (see FIG. **3**) has been removed, an appropriate source/drain material may be dispose within the opening **148** (see FIG. **13**) to form a source/drain structure **184**, as shown in FIG. **14**. As can be seen from FIG. **14**, the dimensions of the source/drain structure **184** are substantially constrained by the dimensions of the original non-planar transistor fin **112**, which may not be optimal for the performance of the non-planar transistor **100** (see FIG. **1**).

Thus, the non-planar transistor fin spacers **146** may be removed prior to the formation of a source/drain structure. As shown in FIG. **15**, a non-directional etch (shown by arrows **192**) may be performed on the non-planar transistor gate spacers **144** and the non-planar transistor fin spacers **146**. As known to those skilled in the art, a non-directional etch may etch all exposed surfaces of the material to be etched at substantially the same rate. As the non-directional etch **172** etches exterior surfaces **146***a*, as well as the interior surfaces **146***b* (i.e. within opening **148**) of the non-planar transistor fin spacers **146**, the non-planar transistor fin spacers **146** are etched away at a faster rate than the non-planar transistor gate spacers **144**, which only etches exterior surfaces **144***a* thereof. Thus, as shown in FIG. **16**, the non-planar transistor fin spacers **146** (see FIG. **15**) may be removed, while the non-planar transistor gate spacers **144** may be merely thinned, but still present. Once the non-planar transistor fin spacers **146** (see FIG. **15**) are removed, as shown in FIG. **16**, the source/drain structure **182** may be formed, as shown and discussed with regard to FIG. **12**.

An embodiment of one process of forming a non-planar transistor of the present description is illustrated in a flow diagram **200** of FIG. **17**. As defined in block **210**, a non-planar transistor fin may be formed on a substrate. A non-planar transistor gate may be formed over the non-planar transistor fin, as defined in block **220**. A dielectric material layer may be conformally deposited over the non-planar transistor gate and non-planar transistor fin, as defined in block **230**. As defined in block **240**, a portion of the dielectric material layer adjacent the non-planar transistor gate may be formed into spacers. A portion of the dielectric material adjacent the non-planar transistor fin may be removed simultaneously with the formation of the non-planar transistor gate spacers, as defined in block **250**. A non-planar source/drain structure then may be formed, as defined in block **260**.

An embodiment of one process of forming a non-planar transistor of the present description is illustrated in a flow diagram **300** of FIG. **18**. As defined in block **310**, a non-planar transistor fin may be formed on a substrate. A non-planar transistor gate may be formed over the non-planar transistor fin, as defined in block **320**. A dielectric material layer may be conformally deposited over the non-planar transistor gate and non-planar fin, as defined in block **330**. As defined in block **340**, a portion of the dielectric material layer adjacent the non-planar gate may be formed into non-planar gate spacers and a portion of the dielectric material layer adjacent the non-planar transistor fin may be simultaneously formed into non-planar fin spacers. The non-planar transistor fin may be removed, as defined in block **350**. As shown in block **360**, the non-planar transistor fin spacers may be removed after the removal of the non-planar transistor fin. A non-planar source/

drain structure may be formed after the removal of the non-planar transistor fin spacers, as shown in block **370**.

It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGS. **1-18**. The subject matter may be applied to other microelectronic device fabrication applications, as will be understood to those skilled in the art. Furthermore, the subject matter may also be used in any appropriate application outside of the microelectronic device fabrication field.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

What is claimed is:

1. A method comprising:

forming a non-planar transistor fin on a substrate;

forming a non-planar transistor gate over the non-planar transistor fin;

conformally depositing a dielectric material layer over the non-planar transistor gate and the non-planar transistor fin; and

forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent sidewalls of the non-planar transistor gate; and

removing the dielectric material layer adjacent the non-planar transistor fin;

wherein forming the non-planar transistor gate spacers and removing the dielectric material layer adjacent the non-planar transistor fin occur simultaneously;

wherein forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent sidewalls of the non-planar transistor gate, and removing the dielectric material layer adjacent the non-planar transistor fin comprises:

forming a capping structure on a portion of the dielectric material layer proximate an upper portion of the non-planar transistor gate, comprising:

forming a sacrificial layer on the dielectric material layer;

recessing the sacrificial layer to expose a portion of the dielectric material layer;

altering the etching characteristics of the exposed portion of the dielectric material layer;

removing the sacrificial layer; and removing the unaltered portion of the dielectric material layer; and

directionally etching a portion of the dielectric material layer adjacent the non-planar transistor fin.

2. The method of claim **1**, wherein altering the etching characteristics of the exposed portion of the dielectric material layer comprises ion doping the exposed portion of the dielectric material layer.

3. The method of claim **2**, further comprising annealing the ion doped portion of the dielectric material layer.

4. The method of claim **1**, further comprising forming a source/drain structure adjacent the non-planar transistor gate.

5. The method of claim **4**, wherein forming a source/drain structure comprising implanting a portion of the non-planar transistor fin with a dopant.

6. The method of claim **5**, wherein implanting a portion of the non-planar transistor fin with a dopant comprises implanting the portion of the non-planar transistor fin with a P-type dopant.

7. The method of claim **5**, wherein implanting a portion of the non-planar transistor fin with a dopant comprises implanting the portion of the non-planar transistor fin with an N-type dopant.

8. The method of claim **4**, wherein forming a source/drain structure comprises removing a portion of the non-planar transistor fin and replacing the same with a source/drain structure.

9. The method of claim **8**, wherein replacing the source/drain structure comprises epitaxially forming a silicon-containing source/drain structure.

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